CLAIMS

1. A semiconductor package containing an integrated-circuit chip, the semiconductor package comprising:

a leadframe formed from spaced-apart electrical connection leads;

an integrated-chip fixed to a front surface of the electrical connection leads;

electrical connection means for connecting the integrated-chip to the electrical connection leads; and

a block of an encapsulation material into which at least a portion of the electrical connection leads are embedded.

2. The semiconductor package according to claim 1, wherein one or more of the electrical connection leads have at least one rear external electrical connection surface which is not covered by the encapsulation.

3. The semiconductor package according to claim 2, wherein one or more of the electrical connection leads have at least one rear external electrical connection surface which is not covered by the encapsulation material so as to form a rear face of a semiconductor package.

4. The semiconductor package according to claim 1, wherein the electrical connection leads have one or more rear recesses covered by the encapsulation material.

5. The semiconductor package according to claim 1, wherein one or more of the electrical connection leads have an end part that extends along a rear face of the integrated-chip and wherein the integrated-chip is fixed to an upper surface of the rear face.

6. The semiconductor package according to claim 5, wherein the integrated-chip is fixed to the electrical connection leads via an adhesive film.

7. The semiconductor package according to claim 1, wherein the electrical connection means further comprises one or more electrical connection wires that electrically connect the integrated-chip to the front surface of the electrical connection leads.

8. The semiconductor package according to claim 1, wherein the integrated-chip and the electrical connection means are embedded in the block of the encapsulation material.

9. The semiconductor package according to claim 1, wherein the integrated-chip is fixed to the electrical connection leads via one or more electrical connection balls.

10. The semiconductor package according to claim 1, wherein the encapsulation block further comprises a forward-projecting peripheral wall forming an annular wall.

11. The semiconductor package according to claim 1, wherein the integrated-chip is fixed to a rear face of a plate via first electrical connection balls,

wherein the plate is fixed to a front face of the electrical connection leads via second electrical connection balls, and

wherein the first electrical connection balls and the second electrical connection balls are connected via electrical connection tracks formed on the rear face of the plate.

12. The semiconductor package according to claim 1, wherein the encapsulation block further comprises:

a forward-projecting peripheral wall forming an annular wall which extends a distance from the plate, and

a ring made of a filling material that fills a space which separates a periphery of the plate from the annular wall.

13. The semiconductor package according to claim 12, wherein the integrated-chip further comprises an optical sensor on a front face of the integrated-chip and wherein the plate is transparent.

14. The semiconductor package according to claim 13, further comprising:

an optical device comprising a lens placed above the plate facing the optical sensor.

15. The semiconductor package according to claim 14, wherein the optical device further comprises an annular support fixed to the annular wall.

16. The semiconductor package according to claim 15, wherein the annular support is adhesively bonded to the annular wall via the ring of filling material.

17. The semiconductor package according to claim 1, further comprising:

a wall formed by the electrical connection leads and at least partly the block of encapsulation material; and

one or more front electrical connection surfaces for connecting the integrated-chip, wherein the front electrical connection surfaces are not covered by the encapsulation material;

wherein the encapsulation material fills one or more spaces formed between the electrical connection leads with rear external electrical connection leads surfaces not covered by the encapsulation material, and the electrical connection leads with rear external electrical connection leads surfaces covered by the encapsulation material.

18. The semiconductor package according to claim 5, further comprising:

a wall formed by the electrical connection leads and at least partly the block of encapsulation material; and

one or more front electrical connection surfaces for connecting the integrated-chip, wherein the front electrical connection surfaces are not covered by the encapsulation material;

wherein the encapsulation material fills one or more spaces formed between

the electrical connection leads with rear external electrical connection leads surfaces not covered by the encapsulation material, and the electrical connection leads with rear external electrical connection leads surfaces covered by the encapsulation material.

19. The semiconductor package according to claim 11, further comprising:

a wall formed by the electrical connection leads and at least partly the block of encapsulation material; and

one or more front electrical connection surfaces for connecting the integrated-chip, wherein the front electrical connection surfaces are not covered by the encapsulation material;

wherein the encapsulation material fills one or more spaces formed between the electrical connection leads with rear external electrical connection leads surfaces not covered by the encapsulation material, and the electrical connection leads with rear external electrical connection leads surfaces covered by the encapsulation material.

20. The semiconductor package according to claim 16, further comprising:

a wall formed by the electrical connection leads and at least partly the block of encapsulation material; and

one or more front electrical connection surfaces for connecting the integrated-chip, wherein the front electrical connection surfaces are not covered by the encapsulation material;

wherein the encapsulation material fills one or more spaces formed between the electrical connection leads with rear external electrical connection leads surfaces not covered by the encapsulation material, and the electrical connection leads with rear external electrical connection leads surfaces covered by the encapsulation material.